REMARKS

Claims 1-2, 4-12, 14-22, 24-31 and 33-38 are rejected under 35 USC 103(a) as being unpatentable over Baird (USP 6,753,738) in view of Carroll (USP 5,130,571), prior art of record

Applicants assert that claims 1-2, 4-12, 14-22, 24-31 and 33-38 should not be found rejected under 35 USC 103(a) as being unpatentable over Baird (USP 6,753,738) in view of Carroll (USP 5,130,571) because there is no motivation to combine the above cited references. In addition to all the reasons against the desirability of combining the above cited references previously provided by the applicants in the first response to the above rejection (see applicants' previous response dated 02/22/2006), applicants further provide the following showing how there is a lack of any motivation to combine the above references in the way stated by the Examiner.

Applicants have found that the definition of "perturbation" in Baird's US6753738 is an important factor. In particular, applicants point out that the perturbation mentioned in Baird's US6753738 is not related to the clock feedthrough (charge injection) problem. In the detailed description for '738 (col 6, starting on line 35), "The switch select signals SELECT<35:0> are preferably driven with a 'one-hot' coding so that, at most, only one individual variable capacitance circuit 272.i is connected to the DAC 268 and is potentially changing in value at any given time. However, other schemes are possible. For example, two or more such individual variable capacitance circuits 272.i could be driven at the same time with a gate control voltage having a slowly-changing voltage magnitude, although the perturbation to the VCO 136 may be more significant."

By switching only one such slow digital control signal V_{SD} <i> at a time, then only one such pair of switching transistors (e.g., transistors 302.0, 303.0) is partially turned on at a time, and the resulting conductance peak described earlier (i.e., in respect to FIG. 4E) only occurs in a single transistor pair during its turn-on or turn-off transient. Moreover, the slow digital control circuit 306 is preferably configured to provide a very slow rise time and fall time on

whichever slow digital control signal V_{SD} <i> changes logic state at any given time, while holding all other slow digital control signals quiescent at one of the static levels. This allows the value of the total capacitance to change much more slowly and reduces perturbations to the overall system.

This results in an extremely slow change in the resistance of the digital portion of the replica termination resistor 439, which affords the feedback loop based upon the amplifier circuit 442 (and to a lesser extent, operational amplifier 434) time to compensate for this change in resistance even during the (preferably slow) transition time of the digital gate control signals 438.i. In other words, the analog loop is fast enough that the total resistance value of the replica termination resistor 439 remains substantially constant even as its digital portion switches. As a result, the input termination resistor 412 value remains constant as the underlying resistor parameters drift, yet without any noticeable perturbations or transient effects which might otherwise disrupt the signal integrity of the incoming data input signal.

From the above description, applicants believe the said perturbation refers to "the variation situation/speed of the capacitance". In other words, applicants believe that "change much more slowly" and "reduces perturbations" mean the same thing. From this angle, one can then realize why the inventor preferred "... only one individual ...., two or more ... although the perturbation to the VCO 136 may be more significant " as stated above (col 6, starting on line 35). Applicants do not believe the perturbation mentioned in Baird's US6753738 is related to the clock feedthrough (charge injection problem), since '738 did not mention it at all. Although the method is similar, Baird did not teach such a method can solve the clock feedthrough issue.

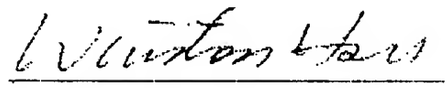
Another import point is, the clock feedthrough problem that the present invention is concerned with is much more serious when the switched capacitor circuit is turned off rather than turned on. Unlike this situation, the "perturbation" cared by Baird is both for "turn on" and "turn off", and especially "turn on" is its example as stated above. This again proves that the said perturbation has nothing to do with the clock feedthrough effect.

Yet another import point is to deal with the "resistance" as stated above, which is used to

prevent said perturbation, however cannot deal with the clock feedthrough problem at all. From this viewpoint, it is understood that the said perturbation mentioned in '738 should be uncorrelated with the clock feedthrough issue.

Based on the above arguments in addition to all the reasons against the desirability of combining the references provided by the applicants in the previous response to the above rejection (see applicants' previous response dated 02/22/2006), applicants assert there is no motivation for one skilled in the art to combine these two cited patents and result in the present invention. Therefore, applicant asserts claims 1-2, 4-12, 14-22, 24-31 and 33-38 should be found allowable with respect to Baird (USP 6,753,738) in view of Carroll (USP 5,130,571), prior art of record. Reconsideration of claims 1-2, 4-12, 14-22, 24-31 and 33-38 is respectfully requested.

Sincerely yours,



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Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

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PAGE 7/7 * RCVD AT 6/27/2006 2:39:43 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/7 * DNIS:2738300 * CSID:18064986673 * DURATION (mm-ss):03-04